Docket No. 29936/39865

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR UNITED STATES LETTERS PATENT

Title:

INPUT AND OUTPUT DRIVER

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INPUT AND OUTPUT DRIVER

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to an input and output driver and, more specifically, to an input and output driver capable of effectively reducing an input capacitance Cin of a DDR-Ⅲ product.

2. Discussion of Related Art

[0002] Double data rate (DDR)-Ⅲ standard graphic DRAM products require a channel impedance of 40Ω in which at least 30Ω tuning is supported. Furthermore, an on-die termination (ODT) circuit, which is provided in a GDRAM in order to match impedance between a graphic processor unit (GPU) and a graphic DRAM (GDRAM), requires impedance of about 60Ω . Furthermore, in the GDRAM, the input capacitance Cin is limited to 3pF or less to insure transmission of signal wave forms at the time of high-speed operation of 700MHz level.

[0003] Generally, a DQ pin for transmitting and receiving data is connected to complex circuit elements, such as an input buffer, an output driver, an electrostatic discharge protection circuit (herein after, referred to as "ESD"), and an ODT circuit. Thus, the input capacitance Cin including a capacitance component due to a package is easily over 3pF. Accordingly, improvement in the field of elements or processes is required.

[0004] Furthermore, increase in the capacitance due to an ODT switch transistor necessary for the ODT circuit makes it very difficult to satisfy requirements for the input capacitance Cin. The more increased a memory operation frequency is, the more decreased a maximum allowable value of the input capacitance is. Therefore, in order to reduce the input capacitance Cin, synthetic improvement, such as improvement of design approach in addition to decrease in relevant processes and design rules, are required.

SUMMARY OF THE INVENTION

[0005] Therefore, the present invention is contrived to solve the aforementioned problems in the art, and the present invention is directed to an input and output driver capable of effectively reducing an input capacitance Cin of a DDR-Ⅲ product.

[0006] According to a preferred embodiment of the present invention, there is provided an input and output driver capable of effectively reducing an input capacitance Cin of a DDR-Ⅲ product as well as satisfying ODT operation conditions requirements specified in a DDR-Ⅲ product standard.

[0007] One aspect of the present invention is to provide an input and output driver comprising: an input buffer for supplying an input data from a DQ pad to a memory cell array in a writing mode; an output driver for supplying an output data from the memory cell array to the DQ pad in a reading mode; and a DQ switch for electrically isolating the output driver from the DQ pad in the writing mode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The above and other objects, advantages and features of the present invention will become apparent from the following description of preferred embodiments given in conjunction with accompanying drawings, in which:

[0009] Fig. 1 is a block diagram of an input and output driver according to a preferable embodiment of the present invention.

[0010] Figs. 2A to 2C are detailed circuit diagrams of a DQ switch shown in Fig. 1.

[0011] Fig. 3 is a view illustrating variation in linearity of a resistance depending on a voltage supplied to a DQ switch shown in Fig. 1.

[0012] Fig. 4 is a circuit diagram illustrating an operation characteristic of an LVT NMOS transistor shown in Fig. 2A.

[0013] Fig. 5 is a circuit diagram illustrating an operation characteristic of a transfer gate shown in Fig. 2C.

[0014] Fig. 6 is a circuit diagram of the input and output driver including an ODT circuit which the DQ switch shown in Fig. 1 is applied to.

[0015] Fig. 7 is a detailed circuit diagram of the ODT circuit shown in Fig. 6.

[0016] Fig. 8 is a circuit diagram of the input and output driver including an ODT circuit, an ESD circuit, and a CDM circuit, which the DQ switch shown in Fig. 1 is applied to.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0017] According to an aspect of the present invention, an input and output driver comprising: an input buffer for supplying input data from a DQ pad to a memory cell array in a writing mode; an output driver for supplying output data from the memory cell array to the DQ pad in a reading mode; and a DQ switch for electrically isolating the output driver from the DQ pad in the writing mode.

[0018] Now, preferable embodiments of the present invention will be described with reference to accompanying drawings. However, the present invention is not limited to the preferred embodiments disclosed in the following description, but can be implemented into various changes and modifications. Thus, these embodiments according to the invention are for informing those skilled in the art of the scope of the present invention.

[0019] Fig. 1 is a block diagram of an input and output driver according to a preferable embodiment of the present invention.

[0020] Referring to Fig. 1, an input and output driver according to a preferred embodiment of the present invention comprises an input buffer 10, an output driver 20, and a DQ switch 30, and is connected to a DQ pad 40.

[0021] In a writing mode, the DQ switch 30 is turned-off to electrically isolate the output driver 20 from the DQ pad 40. On the other hand, in a reading mode, the DQ switch 30 is turned-on to electrically connect the output driver 20 to the DQ pad 40.

[0022] In the writing mode, the DQ switch 30 is tuned-off to electrically isolate the output driver 20 from the DQ pad 40, whereby it is possible to reduce increment in a capacitance due to the output driver 20. In the reading

mode, the DQ switch 30 is turned-on to electrically connect the output driver 20 to the DQ pad 40, whereby the output driver 20 normally outputs data.

[0023] As shown in Fig. 1, in the writing mode, data from the DQ pad 40 is transmitted to a memory cell array (not shown) through the input buffer 10. As a result, in the writing mode, writing operation is performed through the input buffer 10 regardless of operation of the output driver 20. Therefore, in the writing mode, the input and output driver according to a preferred embodiment of the present invention electrically isolates the output driver 20 from the DQ pad 40 using the DQ switch 30. As a result, it is possible to reduce increment in capacitance due to the output driver 20. On the other hand, in the reading mode, data DATAO sensed from the memory cell array is output to the DQ pad 40 through the output driver 20. Therefore, in the reading mode, the DQ switch 30 is turned-on to electrically connect the output driver 20 to the DQ pad 40.

[0024] The DQ switch 30 comprises an LVT (LOW VT) NMOS transistor LNM or an LVT PMOS transistor LPM, as shown in Fig. 2A. For example, a threshold voltage VT of the LVT NMOS transistor LNM or the LVT PMOS transistor LPM is preferably 0.15V or less. In addition, a gate voltage VG of the LVT NMOS transistor LNM is preferably a pumping voltage VPP (3.5V or more) instead of a power source voltage VDD (1.8V). The pumping voltage VPP is generally twice the power source voltage. On the other hand, a gate voltage of the LVT PMOS transistor LPM is preferably a negative pumping voltage '–VPP' or a ground voltage VSS.

[0025] As described above, a reason for considering the threshold voltage VT and gate voltage VG of the transistor used as the DQ switch 30 (herein after, referred to as "DQ transistor") are as follows. First, if a channel resistance loaded to the DQ transistor becomes extremely large, it is difficult to significantly ensure linearity of the total channel resistance including the channel resistance of the transistor and serial resistances, which constitute the output driver 20. Therefore, it is necessary that a gate width of the DQ transistor is maximized and the threshold voltage of the DQ transistor is minimized to minimize an on-resistance of the DQ transistor. However, since a junction capacitance due to a drain and source junction layer and a gate overlap capacitance generated at an overlapped portion between the gate electrode and the drain and source junction layer may be magnified, it is needed to adjust the gate width of the DQ transistor. Second, linearity of the channel resistance is largely changed depending on the gate voltage VG of the DQ transistor. As shown in Fig. 3, linearity of the channel resistance in the case that the gate voltage VG of the DQ transistor is 0V to the pumping voltage VPP is more excellent than that in the case that the gate voltage VG of the DQ transistor is 0V to the power source voltage VDD. Furthermore, since the threshold voltage causes voltage loss at the time of transferring HIGH signals when the gate voltage VG is the power source voltage VDD, it is preferable that the gate voltage VG is the pumping voltage VPP.

[0026] In addition, the DQ switch 30 may be comprised of a plurality of LVT NMOS transistors (LNM0 to LNMn) connected in parallel to minimize the channel resistance loaded to the DQ transistor, as shown in Fig. 2B.

Similarly, the DQ switch 30 may be comprised of a plurality of LVT PMOS transistors (not shown) connected in parallel. At that time, since the total capacitance may be extremely magnified when the DQ switch 30 is comprised of a plurality of LVT NMOS or PMOS transistors connected in parallel, it is preferable to adjust the number of the LVT NMOS or PMOS transistors. On the other hand, as shown in Fig. 2A, considering linearity of the channel resistance when the DQ switch 30 is comprised of the LVT NMOS transistors LNM or LVT PMOS transistors LPM, it is preferable that the gate voltage VG is the pumping voltage VPP. However, since the used pumping voltage VPP is relatively high, it can make it difficult to design that. Therefore, as shown in Fig. 2C, the DQ switch 30 may be comprised of a transfer gate TM comprising the LVT NMOS transistor and the LVT PMOS transistor connected in parallel. In this case, each gate voltage VG may be the power source voltage VDD. The DQ switch 30 is comprised of the transfer gate TM, whereby it is possible to prevent from a voltage loss in transferring HIGH or LOW signals.

[0027] As described above, it is necessary that the DQ switch 30 is operated to be turned-off in the reading mode and turned-on in the writing mode. The operation of the DQ switch 30 will be described through circuit diagrams shown in Figs. 4 and 5.

[0028] As shown in Fig. 4, when the DQ switch 30 is comprised of an LVT NMOS transistor LNM, a control unit 50 is constructed to operate depending on a writing enabling signal WE. The control unit 50 is comprised of a PMOS transistor PM and an NMOS transistor NM connected in serial. Inspecting the operation characteristic of the control unit, the NMOS transistor

NM is turned-on and the PMOS transistor PM is turned-off depending on a writing enabling signal WE, which is enabled (HIGH level) in the writing mode. Accordingly, LVT NMOS transistor LNM is turned-off, whereby the output driver 20 is electrically isolated from the DQ pad 40. On the other hand, the NMOS transistor NM is turned-off and the PMOS transistor PM is turned-on depending on a writing enabling signal WE which is disenabled (LOW level) in the reading mode. Accordingly, LVT NMOS transistor LNM is turned-on, whereby the output driver 20 is electrically connected to the DQ pad 40.

[0029] Furthermore, as shown in Fig. 5, when the DQ switch 30 is comprised of the transfer gate TM, first and second control units 60a and 60b are constructed to operate depending on the writing enabling signal WE. The first control unit 60a is comprised of a PMOS transistor PM1 and an NMOS transistor NM1 connected in serial. The second control unit 60b is comprised of a PMOS transistor PM2 and an NMOS transistor NM2 connected in serial. Inspecting the operation characteristics of the control units 60a and 60b, the NMOS transistor NM1 is turned-on and the PMOS transistor PM1 is turned-off, and simultaneously the NMOS transistor NM2 is turned-on and the PMOS transistor PM2 is turned-off, depending on the writing enabling signal WE which is enabled in the writing mode. Accordingly, both of the NMOS transistor and the PMOS transistor in the transfer gate TM are turned-off, whereby the output driver 20 is electrically isolated from the DQ pad 40. On the other hand, the NMOS transistor NM1 is turned-off and the PMOS transistor PM1 is turned-on, and simultaneously the NMOS transistor NM2 is

turned-off and the PMOS transistor PM2 is turned-on, depending on the writing enabling signal WE which is disenabled in the reading mode,. Accordingly, both NMOS transistor and PMOS transistor of the transfer gate TM are turned-on, whereby the output driver 20 is electrically connected to the DQ pad 40.

[0030] Generally, as shown in Fig. 6, in order to match impedance between a GPU 200 and a GDRAM 100, an ODT circuit 70 is provided in a GDRAM 100. The ODT circuit 70 requires an impedance of 60Ω . In the input and output driver according to the preferable embodiment of the present invention, the ODT circuit 70 is provided between a voltage source and a node N which is connected to the DQ switch 30 and the DQ pad 40. Specifically, as shown in Fig. 7, the ODT circuit 70 is connected between the node N and the voltage source for supplying the power source voltage VDD. The ODT circuit 70 is comprised of an ODT switch ODTS and an ODT resistor ODTR. The ODT switch ODTS is controlled by control signals GPUCA of the GPU 200. Furthermore, as shown in Fig. 8, the input and output driver further comprises an ESD circuit 80 and a charged device model CDM 90 in addition to the ODT circuit 70. The ESD circuit 80 comprised of ESD transistors ESDU and ESDD connected in serial is provided between the DQ pad 40 and the CDM circuit 90. The CDM circuit 90 comprised of a CDM transistor CDMT and a CDM resistor CDMR is provided between the input buffer 10 and the ESD circuit 80.

[0031] As shown in Fig. 8, in the writing mode, the total input capacitance Cin of the input and output driver according to the preferable

embodiment of the present invention is sum of junction layer capacitances and gate overlapped capacitances of the ODT switches ODTS of the input buffer 10, the CDM circuit 90, the ESD circuit 80, and the ODT circuit 70 and the DQ switch 30. In addition to the aforementioned capacitances, the total input capacitance further includes a capacitance due to a package and interconnection capacitances of signal metal lines. Since the input and output driver according to the preferable embodiment further comprises the DQ switch 30, the junction layer capacitances and the gate overlap capacitances of the transistors constituting the DQ switch 30 are increased, in comparison with the conventional input and output driver which has no DQ switch 30. However, in the writing mode, since the output driver 20 is electrically isolated from the DQ pad 40 using the DQ switch 30, the total input capacitance Cin is decreased. The more significant reason is that the capacitance increased by the junction layer capacitances and the gate overlapped capacitances of the output driver 20 is extremely larger than that increased by the DQ switch 30. This will be described with reference to table 1 as follows.

[Table 1]

DQ pin [pF]	ESD circuit	CDM circuit	Output driver	ODT circuit	DQ switch	package	Others	total
DQ switch not used	0.600	0.050	0.565	0.305	0.000	1.070	0.500	3.090
DQ switch used	0.600	0.050	0.000	0.305	0.176	1.070	0.500	2.701

[0032] Table 1 represents values of input capacitance Cin calculated in the input and output driver circuit designed to satisfy the DDR-Ⅲ standard for GDRAM. As shown in table 1, by using the DQ switch, the input capacitance Cin of 0.39pF (12.6%) is reduced. As a result, the input and output driver circuit satisfies a condition of the input capacitance Cin of the DDR-Ⅲ standard for GDRAM.

[0033] In the aforementioned description, although spirit of the present invention has been described in detail using the preferable embodiments, the preferable embodiments will be provided for more complete explanation of the present invention to those skilled in the art. Therefore, it is noted that the present invention is not limited to the embodiments. However, it is understood that various changes and modifications may be made to the embodiments by those who skilled in the art without departing from the spirit of the present invention.

[0034] As described above, according to the present invention, it is possible to reduce the total input capacitance Cin by electrically isolate the output driver from the DQ pad using the DQ switch in the writing mode to reduce the capacitance due to the output driver.

[0035] Furthermore, it is possible to effectively reduce the input capacitance Cin as well as to satisfy an ODT operation condition of the DDR-Ⅲ standard by providing the ODT circuit and the DQ switch to the input and output driver according to the present invention.